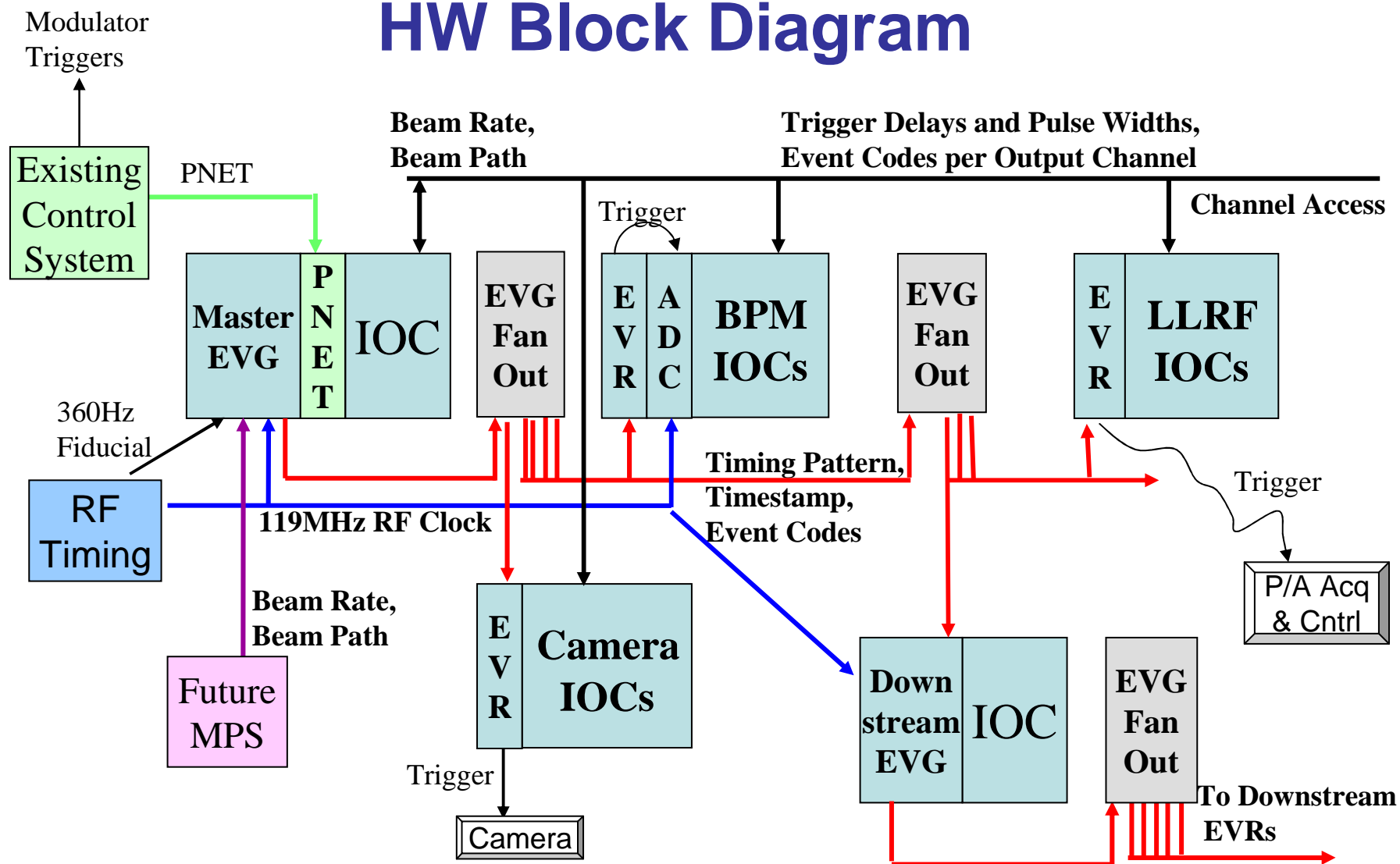


# LCLS Event System

## ■ Outline

- HW Block Diagram
- Timing Requirements
- Time Lines
- EVG to EVR Data Transfer
- Beam-Synchronous Acquisition and Control
- Issues/Comments
- Status/To-Do

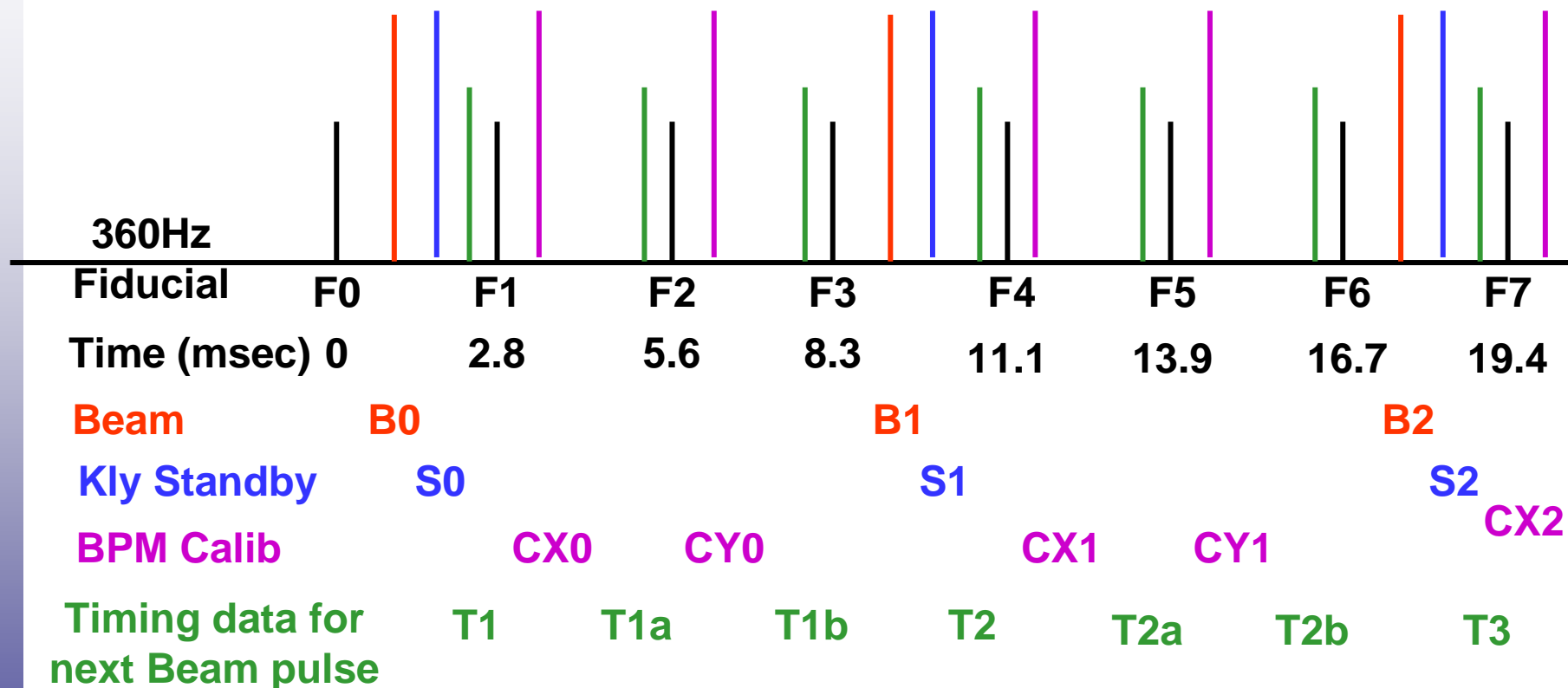
# HW Block Diagram



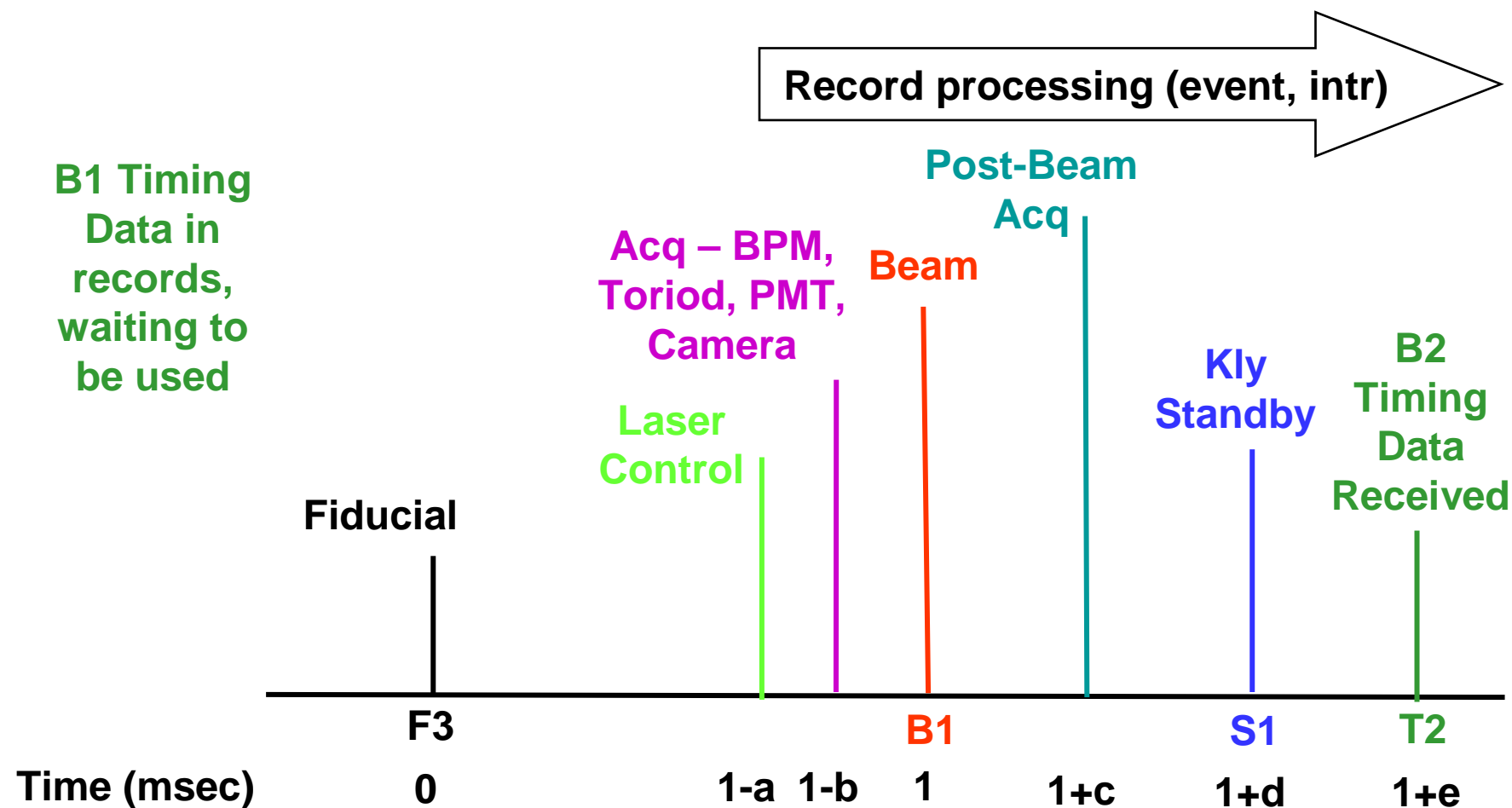
## Timing Requirements

Maximum trigger rate	360 Hz
Clock frequency	119 MHz
Clock precision	20 ps
Coarse step size	8.4 ns $\pm$ 20 ps
Delay range	>1 sec
Fine step size	20 ps
Max timing jitter w.r.t. clock	2 ps rms
Differential error, location to location	8 ns
Long term stability	20 ps

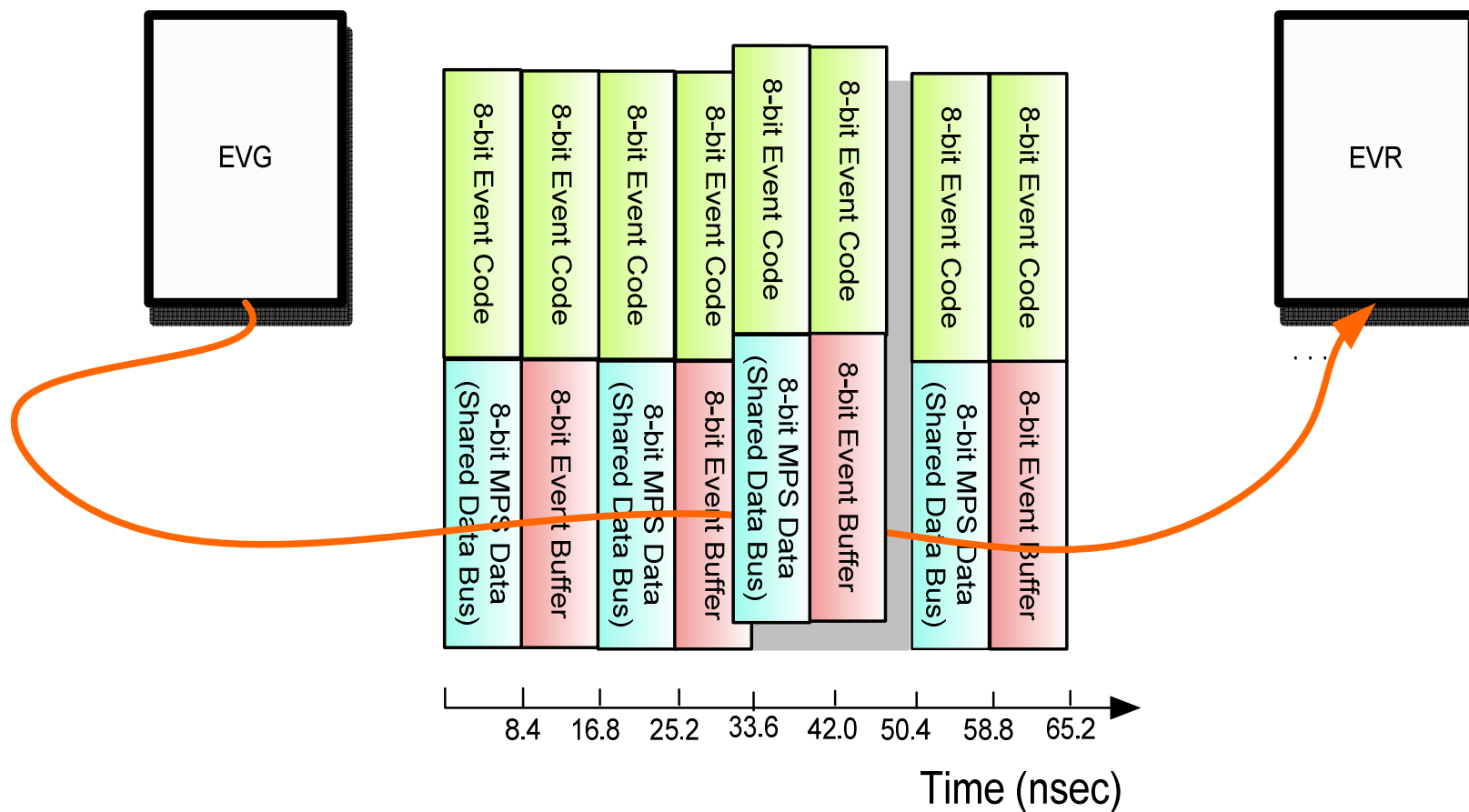
## Event Time Line – 120 Hz Beam



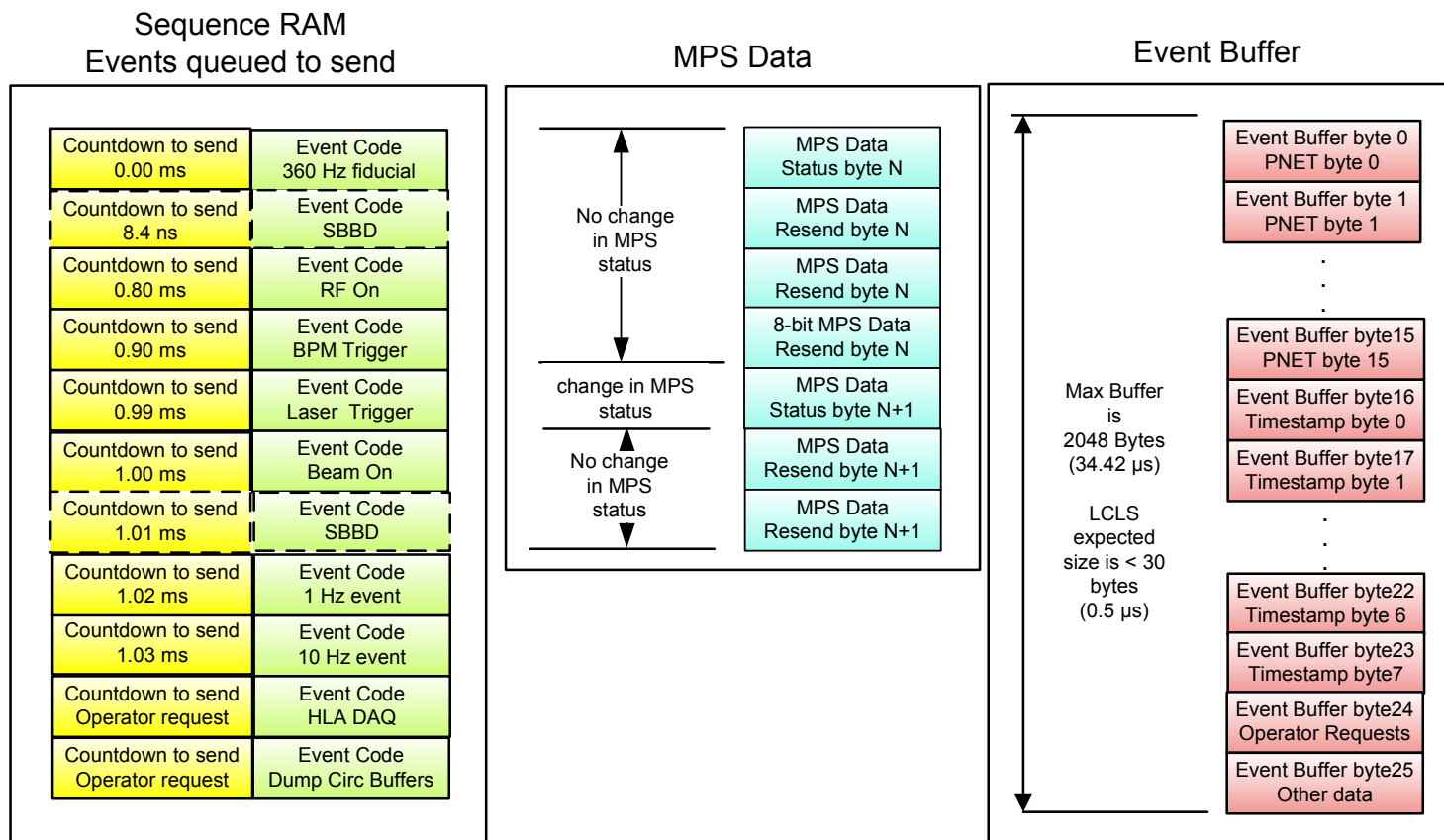
## Event Time Line – 1 Beam Pulse (B1)



## EVG-to-EVR Data Transfer (Dayle Kotturi)

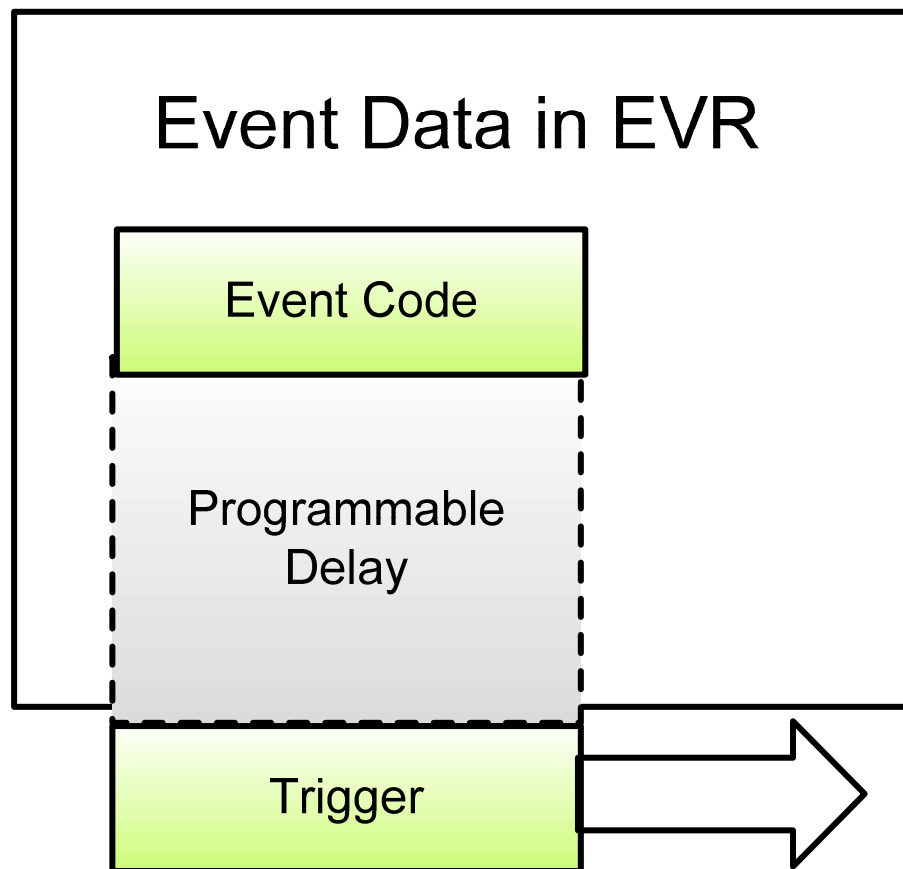


# EVG-to-EVR Data Example (Dayle Kotturi)



Two SBBB event codes shown. First is case to send beam to undulator; second is timed to prevent beam from reaching undulator. It's one OR the other, per seq RAM.

## Trigger from Event Code (Dayle Kotturi)





## Event Applications

- Beam-Synchronous Control: rules and algorithm for creating EVG trigger sequences on a pulse-to-pulse basis
  - Algorithm change on-the-fly based on user requests
    - Single-Shot vs continuous beam pulses – enforce minimum delay between single-shot requests
    - Bunch length measurement
    - Rate limit
    - Beam destination
  - MPS rate limit and destination requests
  - Send out calibration, standby, and software triggers during non-beam time slots

## Event Applications (cont)

- Beam-Synchronous Acquisition: mechanism for users to request pulse-by-pulse acquisition across multiple IOCs:
  - Single-shot or multiple contiguous pulses
  - Include or exclude a pulse from resultant waveforms based on information in the timing pattern for that pulse
  - Can be implemented by either data mining of large data/timing-pattern arrays
  - ...or use the timing system to trigger data copy to special records based on preset conditions, requires reserve/release of special records

# Immediate Issues/Comments

- EVG RF input divider – new circuit added to EVG
- Do we need EVR with RF recovery (EVR with clock)?  
119Mhz availability throughtout?
- Fiber plant:
  - Match network bulk cable where possible
  - Where is single mode fiber needed? Between fanouts? To EVR w/RF recovery?
  - How much EVR daisy-chaining can we do?
  - Daisy chain vs tap to split
  - No plans for redundancy
- TTL triggers – long trigger cables need design
- Not enough testing has been done
- Schedule.....

## Future Issues

- Modulator triggers on existing control system – how to rate-limit from new system
- Handling non-LCLS beams – add more beam-pulse-dependent info (ie, bunch charge) to timing pattern for IOC apps
- How to upgrade PMC-EVR firmware

## Status (Dayle Kotturi)

- Received the EVG/EVR 200 series VME hardware (which sends up to 2K data buffer)
- Received the EVR 200 series PMC module
- Adapted driver and device support to:
  - send the PNET data buffer (measured 66  $\mu$ s transfer)
  - be OSI (running on mvme6100, RTEMS4.7)
  - with help from Till Straumann, Eric Bjorklund, Timo Korhonen, Jukka Pietarinen and Bob Dalesio

## Status (cont)

- Stephanie Allison and Mark Crane coming up to speed
- Test stands for HW folks not yet ready
- Rack/cable design for injector/BC1 well underway
- Procurement underway

## To-Do

- Finish PMC-EVR driver and test (share PMC-EVR and VME-EVR driver as much as possible)
- EVG sequence RAM programming at 360 Hz
- EVG rules and algorithm definition for Jan commissioning
- Add support for EVR timing pattern data records (in place well before next beam pulse)
- Jitter testing
- Interface with other subsystems needs review
- Commissioning test plan